

## **REMARKS/ARGUMENTS**

Claims 1-21 are pending and rejected. Claims 1, 2, 9-12, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smith, et al., in view of Alpha Architecture Handbook (“Alpha”), and Colwell, et al. Claims 3-8, 13, 15, 18, and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smith et al. in view of Alpha, Colwell et al., and Rotenburg et al., Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching.

### **Claim Rejections Under 35 U.S.C. §103(a)**

The physical zero register disclosed in Alpha is a zero register that is explicitly dedicated as such by the instruction set architecture. “Register R31 is assigned special meaning by the Alpha architecture.” (Alpha, 3-1, section 3.1.2 entitled “Integer Registers”). As the examiner points out in the office action, Smith et al. teaches a “zero-generating apparatus for use with an instruction set architecture without an r0 register.” If a computer architecture contains a dedicated zero register like the one described in Alpha, then there is no need for and no benefit in having a zero generating apparatus like the one taught in Smith. Alpha and Smith teach two different ways of accomplishing the same objective – zero generation. As the examiner states in the office action, the purpose of a physical zero register like the one taught in Alpha is to eliminate the need for a zeroing instruction, like the one taught in Smith. As evidenced by the examiner’s description of Alpha, Alpha and Smith et al. in fact teach away from combining. Since the Alpha and Smith references cannot be properly combined, the office action fails to make a prima facie case of obviousness as required under 35 U.S.C. §103(a). Applicant respectfully submits that for the reasons above,

claims 1, 14, and 17 are in condition for allowance. Applicant further respectfully submits that claims 2-13, 15-16, and 18-21 are allowable as depending from the allowable independent claims 1, 14, and 17.

Based on the arguments and amendments above, reconsideration and withdrawal of the rejection of claims 1-21 under 35 U.S.C. §103(a) is respectfully requested.

**Request for Allowance**

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

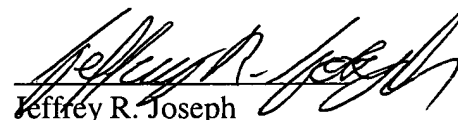
The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: December 13, 2004

By:

  
Jeffrey R. Joseph  
(Reg. No. 54,204)  
Attorneys for Intel Corporation

For:

Shawn W. O'Dowd  
(Reg. No. 34,687)

KENYON & KENYON  
333 West San Carlos St., Suite 600  
San Jose, CA 95110

Telephone: (408) 975-7500  
Facsimile: (408) 975-7501

54273\_1